CLAIMS

What is claimed is:

1. A method for fabricating a window ball grid array (WBGA) semiconductor package, comprising the steps of:

preparing a core layer, the core layer having a first surface and an opposite second surface, and a through hole penetrating through the core layer, wherein the second surface is formed with a plurality of wire-bonding portions around the through hole, a plurality of ball-bonding portions, and a plurality of intended-exposing regions around the wire-bonding portions;

applying a solder mask layer over the second surface of the core layer while exposing the ball-bonding portions, wherein the solder mask layer is formed with an opening for exposing the through hole, the wire-bonding portions, and the intended-exposing regions;

preparing at least one chip which is mounted on the first surface of the core layer and over the through hole, with a portion of the chip exposed via the through hole;

forming a plurality of bonding wires which penetrate through the through hole and electrically connect the chip to the wire-bonding portions;

performing a molding process to form a first encapsulation body on the first surface of the core layer to encapsulate the chip, and a second encapsulation body on the second surface of the core layer to encapsulate the bonding wires, wherein the intended-exposing regions serve as a narrow runner for an encapsulating material forming the second encapsulation body; and

depositing a plurality of solder balls on the ball-bonding portions.

2. The method of claim 1, wherein a width of the intended-exposing region is of a range from 0.2 to 0.8 mm.

3. The method of claim 2, wherein the width of the intended-exposing region is 0.4 mm.

4. The method of claim 1, wherein the intended-exposing regions are located adjacent to the wire-bonding portions.
5. The method of claim 1, wherein the opening of the solder mask layer is larger in width than a mold cavity of a mold used for forming the second encapsulation body.
6. The method of claim 1, wherein the encapsulating material forming the second encapsulation body is filled in the narrow runner to allow the second encapsulation body covering the intended-exposing regions to have a thickness substantially equal to that of the solder mask layer.
7. The method of claim 1, further comprising: applying a layer of patterned conductive traces between the second surface of the core layer and the solder mask layer.
8. The method of claim 1, further comprising: applying another solder mask layer between the first surface of the core layer and the chip.
9. A window ball grid array (WBGA) semiconductor package, comprising:

a core layer having a first surface and an opposite second surface, and a through hole penetrating through the core layer, wherein the second surface is formed with a plurality of wire-bonding portions around the through hole, a plurality of ball-bonding portions, and a plurality of intended-exposing regions around the wire-bonding portions;

at least one chip mounted on the first surface of the core layer and over the through hole, with a portion of the chip exposed via the through hole;

a solder mask layer applied over the second surface of the core layer with the ball-bonding portions being exposed, wherein the solder mask layer is formed with an opening for exposing the through hole, the wire-bonding portions, and the intended-exposing regions;

a plurality of bonding wires which penetrate through the through hole and

electrically connect the chip to the wire-bonding portions;

a first encapsulation body formed on the first surface of the core layer for encapsulating the chip;

a second encapsulation body formed on the second surface of the core layer for encapsulating the bonding wires and the intended-exposing regions; and

a plurality of solder balls deposited on the ball-bonding portions.

10. The WBGA semiconductor package of claim 9, wherein a width of the intended-exposing region is of a range from 0.2 to 0.8 mm.

11. The WBGA semiconductor package of claim 10, wherein the width of the intended-exposing region is 0.4 mm.

12. The WBGA semiconductor package of claim 9, wherein the intended-exposing regions are located adjacent to the wire-bonding portions.

13. The WBGA semiconductor package of claim 9, wherein the opening of the solder mask layer is larger in width than a mold cavity of a mold used for forming the second encapsulation body.

14. The WBGA semiconductor package of claim 9, wherein a thickness of the second encapsulation body covering the intended-exposing regions is substantially equal to that of the solder mask layer.

15. The WBGA semiconductor package of claim 9, further comprising: a layer of patterned conductive traces applied between the second surface of the core layer and the solder mask layer.

16. The WBGA semiconductor package of claim 9, further comprising: another solder mask layer applied between the first surface of the core layer and the chip.

17. A chip carrier used in a window ball grid array (WBGA) semiconductor package, comprising:

a core layer having a first surface and an opposite second surface, and a through hole penetrating through the core layer;

a conductive trace layer applied over the second surface of the core layer, and formed with a plurality of wire-bonding portions around the through hole, a plurality of ball-bonding portions, and a plurality of intended-exposing regions around the wire-bonding portions; and

a solder mask layer applied over the conductive trace layer with the ball-bonding portions being exposed, and formed with an opening for exposing the through hole, the wire-bonding portions, and the intended-exposing regions.

18. The chip carrier of claim 17, wherein a width of the intended-exposing region is of a range from 0.2 to 0.8 mm.

19. The chip carrier of claim 18, wherein the width of the intended-exposing region is 0.4 mm.

20. The chip carrier of claim 17, further comprising: another solder mask layer applied over the first surface of the core layer.